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Title: METHOD AND APPARATUS FOR USING A DEVELOPMENT PORT FOR BOOT UP

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

Enclosed for filing with the above-identified utility patent application, please find the following:

1.	[X]	Specification (Total Pages of Text, including Abstract and Claims: 14)
2.	[X]	Drawing(s) (35 USC 113) (Total Sheets:) [] FORMAL [x] INFORMAL
3.	[X]	Oath or Declaration (Total Pages: 5) [x] Signed [] Unsigned
4.	[]	Microfiche Computer Program (Appendix)
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11.	[]	Copies of IDS Citations (Number of References:)
12.	[]	Preliminary Amendment
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SIGNATURE: Maisie C. Livengood

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TOTAL CLAIMS:	18	-	20	0	X $9 =		OR	X $18 =	$0.00
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Date: 2/5/2000

METHOD AND APPARATUS FOR USING A DEVELOPMENT PORT FOR BOOT UP

The present invention is related to employing a development port of a microprocessor for boot procedures and in particular to reduce or avoid the need for relying on a read only memory (ROM) or similar device for boot up.

BACKGROUND INFORMATION

It is common for microprocessor-based electronic equipment to include two or more interconnected printed circuit boards, often including a main circuit board having the main controller or microprocessor (often termed the "motherboard") and one or more connected "daughterboards". In many electronic devices, some or all of the daughterboards, may, themselves, be "intelligent", i.e., may have their own programmable controllers, typically microprocessors.

When electronic devices of these types are operated, upon initial power-up (or, in some cases, upon resetting the microprocessors) some or all devices on the boards need to access and/or execute certain microcode or other code or configuration information. Some or all of this code or information may include what is commonly called "boot-up code". Because such boot-up code must be available, (e.g. upon power-up), it is often stored in a read only memory (ROM) device mounted on the same board where the microprocessor is mounted. Although ROM components are commonly provided for this purpose, it is, at least theoretically, possible to use any type of non-volatile memory, such as flash memory, SRAM and the like.

In many situations, providing or mounting a separate ROM (or other non-volatile memory) component on an intelligent daughterboard is a non-optimal approach to providing boot-up code. The mounting of a ROM component on a daughterboard occupies surface area on the board which is often needed for accommodating other components or circuitry (particularly since many daughterboards have relatively small surface area). Furthermore, the ROM components themselves undesirably add to the cost of the daughterboard and the cost of mounting such ROM devices undesirably adds to the cost of board fabrication. ROM devices

undesirably consume power. Furthermore, ROM devices and similar memory devices may be cumbersome or impossible to reprogram, e.g., to accommodate upgrades and the like. Accordingly, it would be useful to provide a system, method and apparatus for use in booting up an intelligent daughterboard while eliminating or reducing the need for mounting a ROM or other nonvolatile memory on the daughterboard.

Cost is often a consideration in designing and implementing electronic devices and, although there are advantages (noted above) to avoiding the need for mounting nonvolatile memory on a daughterboard, the cost for such an approach can be a significant issue. Accordingly, it would be useful to provide a system, method and apparatus to reduce or avoid the need for mounting nonvolatile memory on an intelligent daughterboard in which at least some of the components or features involved are components and features which are already present, e.g. for another purpose.

SUMMARY OF THE INVENTION

The present invention includes the recognition of the existence, nature and/or source of problems in previous approaches, including as described herein. According to one aspect, the development port of a daughterboard microprocessor (which is a port that is normally inactive or not used during power-up, boot-up, reset or during normal operation) is used to facilitate one or more of the boot-up procedures, such as accessing or storing boot-up code, configuration information and the like, originating on (or received from) the motherboard (or other component of the electronic device). In one embodiment, the development port is used only for downloading or accessing the minimum amount of boot code (or the like) needed or useful for initially booting or configuring the daughterboard components. In one embodiment, initial code downloaded, via the development port, includes code as needed for configuring a memory controller and/or other devices permitting operation of a DRAM. Thereafter, additional operating system or other code is imported into daughterboard memory via more conventional routes. In another embodiment, the development port is used for downloading, onto the daughterboard, some or all of the operating system (or the so-called "image") used for normal operation of the daughterboard.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1D are a flow diagram and a block diagram, respectively, depicting procedures and components for boot-up with respect to an intelligent daughter card according to one previous approach;

Figs. 1B and 1E are a flow diagram and a block diagram, respectively, depicting procedures and components for boot-up with respect to an intelligent daughter card according to one previous approach;

Figs. 1C, and 1F are a flow diagram and a block diagram, respectively, depicting procedures and components for boot-up with respect to an intelligent daughter card according to one previous approach;

Fig. 2 is a block and flow diagram depicting components and procedures using a Debug port for testing or Debug purposes according to previous approaches;

Figs. 3A, B and C are block diagrams depicting procedures for daughterboard boot-up according to embodiments of the present invention; and

Fig. 4 is a flow chart depicting steps in a boot-up procedure of an intelligent daughterboard according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Before describing aspects of the present invention, certain previously-used approaches will be described. As depicted in Figs. 1A and 1D, according to at least some previous approaches, upon power up (or reset) of an electronic device 112, an intelligent daughterboard 114 (i.e. having a microprocessor or similar controller 116), which is coupled to a motherboard 118 (typically via an edge connector 122) will have a microprocessor 116 which receives boot code 124 from a non-volatile memory such as a ROM 126 mounted on the daughterboard. In a typical situation, the daughterboard processor 116 includes a serial or other port 128 coupled to a bus 132. However, in typical previous devices, it is necessary to use the boot code 124 to configure the serial port 128 before receiving information from the motherboard 118 over the bus 132. For this reason, in the configuration depicted in Fig. 1D, it is impossible to download the

boot code 124 from the motherboard 118 over the bus 132, since the daughterboard 128 cannot be configured until after the boot code 124 has been accessed. As noted above, the need for providing a nonvolatile memory 126 mounted on the daughterboard 114 undesirably increases costs, occupies board surface area, consumes power, and may make it cumbersome or impossible to provide programming upgrades.

After the boot code 124 is provided from the ROM 126, the port 128 can be configured thus permitting the operating system or "image" to be loaded 134 (Fig. 1A), typically from the ROM 126 (Fig. 1D)(e.g. a PROM or from a flash memory). As described below, in other configurations, the image can be downloaded through the interface between the host and the daughtercard. Thereafter, the microprocessor 116 can be reset and the operating system or image can execute 136 (Fig. 1A).

In the approach of Figs. 1B and 1E, a daughterboard which contains a memory other than (or in addition to) a dynamic random access memory (DRAM) storage device, such as a static random access memory device (SRAM) 138 . In the approach of Fig. 1B, following power up or reset 112 the processor 142 (Fig. 1E) on the motherboard (or "host") 118 provides firmware or microcode image for downloading 144, e.g., via a serial or other bus 146 to the non-DRAM storage device 138 on the daughter card 114 (via an interface between the host and the card). Following the image download, the processor on the daughter card 114 is reset 148 (Fig. 1B), after which it executes the image 152.

Unfortunately, the configuration depicted in Figs. 1B and 1E is not feasible when the target device on the daughter card (for storing the image) is DRAM 154 (as depicted in Fig.1F). In the approach depicted in Figs. 1C and 1F, the DRAM 154, for proper operation, needs to be coupled to or controlled by a memory controller 156 (Fig. 1F) (e.g. to provide it with timing information and the like). A memory controller 156 can be provided externally in hardware (e.g. using a programmable logic device or a field programmable gate array or the like) or, in some cases, may be built-in as part of the microprocessor 116. In either case, however, the memory controller 156 must be typically configured before it can control the DRAM 154. Accordingly, in the configuration of Figs. 1C and 1F, upon power up or reset 112 (Fig. 1C), microcode or configuration information 158 (Fig. 1F) is provided to (or accessed by) the microprocessor 116

from a ROM 126 (or other nonvolatile memory) and then provided 162 to the memory controller 156. Thus, in the embodiment of Fig. 1C, a ROM 126 is used, increasing cost, occupying surface area, consuming power and making it impossible or cumbersome to provide updates. In the approach of Figs. 1C and 1F, after the memory controller has been configured, the image or operating system can be downloaded, e.g. from the motherboard 144 for storage 164 in the DRAM 154. Thereafter, the microprocessor 116 is reset 166 (Fig. 1C) and the image stored in the DRAM 154 is executed 168.

Thus, as can be seen from Figs. 1A through F, in the depicted previous approaches, it was typically necessary to provide some type of non-DRAM, typically non-volatile, memory component or device 126 (Figs, 1D and F), 138 (Fig. 1E) (such as a PROM or an SRAM) on the daughterboard 114. SRAMs and similar devices are generally disadvantagous at least because of their relatively high cost, and power and space requirements.

One aspect of the present invention involves the recognition that a component or feature of many types of microprocessors which is provided for testing or debugging purposes, namely the development port (DP) (sometimes referred to as a "Debug port") can play a role in boot-up of an intelligent daughterboard, in particular, in such a way as to reduce or avoid the need for mounting a ROM component (or other non-volatile memory component) on the daughterboard.

Many types of microprocessors provide a development port or debug port. One example is the development port provided in the Motorola MPC860 microprocessor and described, e.g., in MPC860 Power Quicc™ user's manual, especially at pages 4-1 through 4-12 and 18-22, 18-40, incorporated herein by reference. Regardless of what it may be called in other contexts, as used herein, a development port or Debug port of a microprocessor is a port which does not need configuration, following a power-up or (soft) reset, in order to load or receive data provided at the port. In the present context, a soft reset will cause the image to start executing at the reset vector in DRAM. In the example of the MPC860, the development port is a dedicated serial port which does not need any of the regular system interfaces. In the example of the MPC860, the development port provides a full duplex serial interface. The physical connections for using the development port in the MPC860 include a 10-pin connector. Typically, the development port of a microprocessor is inactive or not used during normal operation of the electronic device and also

is typically inactive or not used during power-up or boot-up procedures in an electronic device. Instead, the development port is generally used during product design or development, testing, debugging and the like. In a typical use, a Debug port 212 (Fig. 2) of a microprocessor 214 is connected, via a ribbon connector, cable or the like, 216 to an external emulator device 218. An example of an external emulator device of a type that can be used in connection with the MPC860, for example, is that sold under the trade name Code TAP™, available from Applied Microsystems Corporation, and described, for example, in "Emulator Installation Guide, Code TAP for the Motorola MPC8XX", particularly pages 1-7, 21-8 and 4-124-11, incorporated herein by reference. An emulator 218 is typically used for testing the above unit, or other development purposes, and is typically not coupled to a Debug port during normal operation of an electronic device by an end user. When an emulator 218 is coupled to a Debug port 212, it is possible to use the emulator 218 to load data to the Debug port 212 and, if desired, it would be possible to use an emulator 218 to download boot code 222 to the Debug port 212.

One aspect of the present invention involves using the Debug port of a daughterboard microprocessor during normal use by an end user and, in particular during normal boot-up, such as following power-on or reset. As depicted in Figs. 3A-C and 4, following power-up or reset 412a,b, (Fig.4) initial boot-up code (or configuration information), which can, in at least one embodiment, include memory controller configuration information, is downloaded 314 (Fig. 3A) from a motherboard 316 to a coupled daughterboard 318 through the development port 322 of the daughterboard microprocessor 324. In the embodiment depicted in Fig. 3A, a bus (or other) communication line 326 is provided between the development port 322 and a connection or interface to the motherboard 316, e.g. through an edge connector 328b. In one embodiment, on the daughterboard 318, the bus 326 comprises a plurality of traces or leads formed on the surface of the printed circuit board 318 in a manner that will understood by those of skill in the art. With respect to the motherboard 316, in one embodiment, a serial peripheral device connection is used, at least during boot up, for providing a path to download information codes, configurations and the like stored on the motherboard (e.g. in a memory device mounted on or coupled to the motherboard).

In the embodiment depicted in Figs. 3A-C, the memory controller 332 is provided as a component of the microprocessor 324, although, as noted above, it is also possible to use the present invention in configurations in which a memory controller is provided as an external device. The information which was downloaded 414 is used to configure 416 the memory controller 322. Once the memory controller 332 has been configured, the DRAM 334 is, at least theoretically, operable. In one embodiment (Fig 3C), following configuration of the memory controller 332, further coding or software, such as an operating system or "image" is downloaded 336 (step 436) through the development port 322 for transfer 338 to the DRAM 334. In another embodiment (Fig 3B), image or other code can be transferred 342 from the motherboard and provided 446 to the DRAM 334 by using a system bus 346 i.e. without using the development port 322 for the transfer of the image or the operating system. In any case, after the operating system or image has been stored in the DRAM 334, the daughterboard microprocessor can be (soft) reset 448 and the image can be executed 452.

As can be seen from Figs. 3A-C, use of the development port 322, as described, makes it possible to provide for configuration or boot up of an intelligent daughterboard in the absence of a need for using a ROM or other non-volatile memory mounted on the daughterboard. The depicted embodiments include a DRAM mounted on the daughterboard, but typically, a DRAM would be provided for use during non-boot up general operation of the daughterboard and accordingly does not represent an additional cost, consumption of power or surface area and the like (compared to the power, surface area and cost needed for non-boot-up operation). As noted above, a Debug port is commonly provided on microprocessors (for other purposes) and thus this component or feature used during embodiments of the present invention also is a component or feature which is already present for other purposes and thus is compatible with providing embodiments of the present invention without the need to design or provide additional components. In at least some embodiments, communication of code or data from the motherboard to the daughterboard development port is performed using the motherboard's serial peripheral device connection, coupling or pathway, also already present (on the motherboard) for another purpose, thus in assisting in avoiding the need for incurring additional design or component costs in order to implement embodiments of the present invention.

In light of the above description a number of advantages of the present invention can be seen. The present invention makes it feasible to achieve configuration and/or boot up of an intelligent daughterboard while reducing or eliminating the need for using and/or mounting a ROM or other non-volatile memory device on the daughterboard. The present invention accordingly can reduce the cost, consumption of surface area and/or consumption of power on the daughterboard, needed for boot up or configuration purposes, e.g. providing additional surface area which can be used mounting other circuitry or components. The present invention effectively makes use of one or more features or components which are provided or used for other purposes, thus making it possible to implement at least some embodiment of the present invention without undue requirements for adding additional components to an electronic device.

The number of variations and modifications of the invention can be used. It is possible to use some aspects of the invention without using others. It is possible to use the development port during daughterboard boot up without using it for configuring a memory controller. The present invention can be used in any of a plurality of different types or categories of electronic devices, including personal computers, work stations, network devices such as routers, switches, bridges, hubs and the like, telecommunications devices or components and the like.

The present invention, in various embodiments, includes components, methods, processes, systems and/or apparatus substantially as depicted and described herein, including various embodiments, subcombinations, and subsets thereof. Those of skill in the art will understand how to make and use the present invention after understanding the present disclosure. The present invention, in various embodiments, includes providing devices and processes in the absence of items not depicted and/or described herein or in various embodiments hereof, including in the absence of such items as may have been used in previous devices or processes, e.g. for improving performance, achieving ease and\or reducing cost of implementation. The present invention includes items which are novel, and terminology adapted from previous and/or analogous technologies, for convenience in describing novel items or processes, do not necessarily retain all aspects of conventional usage of such terminology.

The foregoing discussion of the invention has been presented for purposes of illustration and description. The foregoing is not intended to limit the invention to the form or forms

disclosed herein. Although the description of the invention has included description of one or more embodiments and certain variations and modifications, other variations and modifications are within the scope of the invention, e.g. as may be within the skill and knowledge of those in the art, after understanding the present disclosure. It is intended to obtain rights which include alternative embodiments to the extent permitted, including alternate, interchangeable and/or equivalent structures, functions, ranges or steps to those claimed, whether or not such alternate, interchangeable and/or equivalent structures, functions, ranges or steps are disclosed herein, and without intending to publicly dedicate any patentable subject matter.

What is claimed is:

1. Apparatus for use in boot-up of an electronic device which includes a motherboard and a daughterboard comprising:

first data storage device, accessible to said motherboard, storing daughterboard boot-up code;

a coupler, coupling said daughterboard to said motherboard, defining at least a first data communication path from said motherboard to said daughterboard;

a microprocessor positioned on said daughterboard, wherein said microprocessor includes a development port; and

at least a second communication path, defined on said daughterboard, providing for communication from said coupler to said development port;

wherein said boot-up code can be provided from said storage device, over said first communication path, said coupler and said second communication pathway, to said development port of said microprocessor on said daughterboard.

2. Apparatus, as claimed in Claim 1, wherein said motherboard is configured to download at least said boot-up code, to said development port automatically, in response to a power up or a reset of said electronic device.

3. Apparatus, as claimed in Claim 1, wherein said daughterboard includes a DRAM and a memory controller and wherein said boot-up code includes memory controller configuration information.

4. A method for performing boot-up in an electronic device including a motherboard and a coupled daughterboard, said daughterboard including a microprocessor having a development port, comprising:

automatically downloading at least first boot-up code from said motherboard to said development port, in response to a power-on or reset of said electronic device; and

using said boot-up code, in said microprocessor of said daughterboard, for performing at least a first boot-up operation.

5. A method, as claimed in Claim 4, wherein said boot-up operation includes configuring a port, different from said development port.

6. A method, as claimed in Claim 4, wherein said daughterboard includes a DRAM and a memory controller, and wherein said boot-up operation comprises configuring said memory controller.

7. A method, as claimed in Claim 4, further comprising downloading at least a portion of an operating system for said microprocessor, from said motherboard, using said development port.

8. A method, as claimed in Claim 4, wherein said step of downloading said at least first boot-up code is performed while said daughterboard is coupled to said motherboard.

9. A method, as claimed in Claim 4, wherein said step of downloading said at least first boot-up code is performed in the absence of coupling said development port to an external emulator.

10. A method, as claimed in Claim 4, wherein said first boot-up operation is performed in the absence of storing said boot-up code on a daughterboard non-volatile memory prior to said power-up or reset.

11. Apparatus for performing boot up in an electronic device including a motherboard and a coupled daughterboard, said daughterboard including a microprocessor having a development port, comprising:

means for automatically downloading at least first boot up code from said motherboard to said development port, in response to a power on or reset of said electronic device; and

means for performing at least a first boot-up operation, using said boot-up code, in said microprocessor of said daughterboard .

12. Apparatus, as claimed in Claim 11, wherein said means for performing said first boot-up operation includes means for configuring a port, different from said development port.

13. Apparatus, as claimed in claim 11, wherein said means for performing said first boot-up operation includes means for initializing DRAM chip selects.

14. Apparatus, as claimed in Claim 11, wherein said daughterboard includes a DRAM and a memory controller, and wherein said means for performing said first boot up operation comprises means for configuring said memory controller.

15. Apparatus, as claimed in Claim 11, further comprising means for downloading at least a portion of an operating system for said microprocessor, from said motherboard, using said development port.

16. Apparatus, as claimed in Claim 11, wherein said means for automatically downloading includes means for downloading while said daughterboard is coupled to said motherboard.

17. Apparatus, as claimed in Claim 11, wherein said means for downloading includes means for downloading in the absence of coupling said development port to an external emulator.

18. Apparatus, as claimed in Claim 11, wherein said means for performing said first boot-up operation includes means for performing said first boot-up operation in the absence of

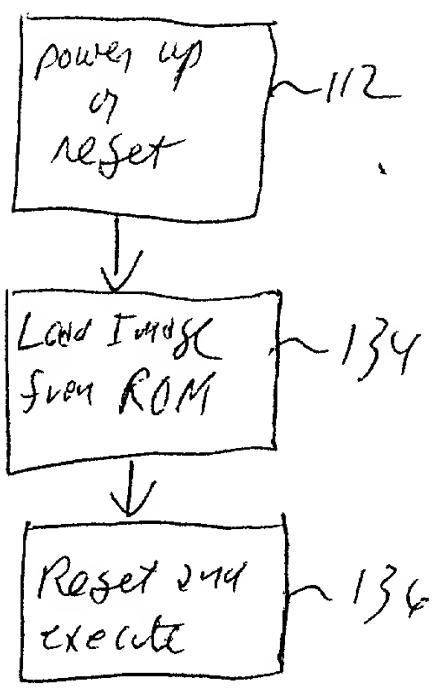
storing said boot-up code on a daughterboard non-volatile memory prior to said power-up or reset.

ABSTRACT

The development port or Debug port of a microprocessor on an intelligent daughterboard is used for downloading code or configuration information from a motherboard for use in boot-up. In various aspects, the code or configuration information can include information used for configuring a port, other than the development port, and/or for configuring a memory controller, such as for a daughterboard DRAM. Use of the Debug port makes it possible to reduce or eliminate the need for storing boot-up code or configuration information on a daughterboard ROM, or other non-volatile memory, thus reducing cost and space requirements, power consumption and the like.

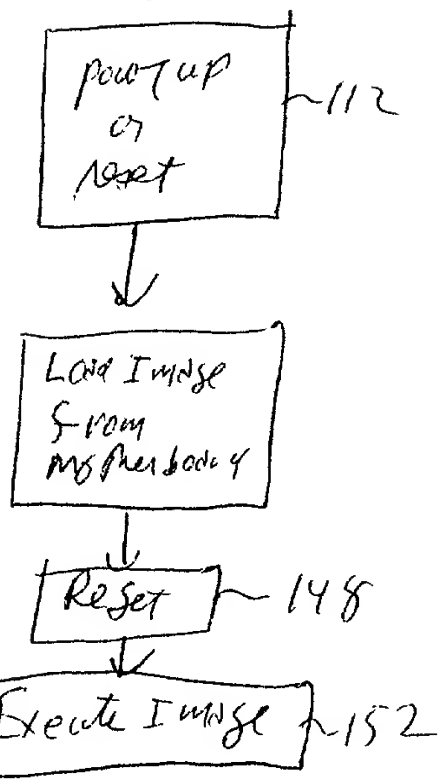
Prior Art

Fig 1A



Prior Art

Fig 1B



Prior Art

Fig 1C

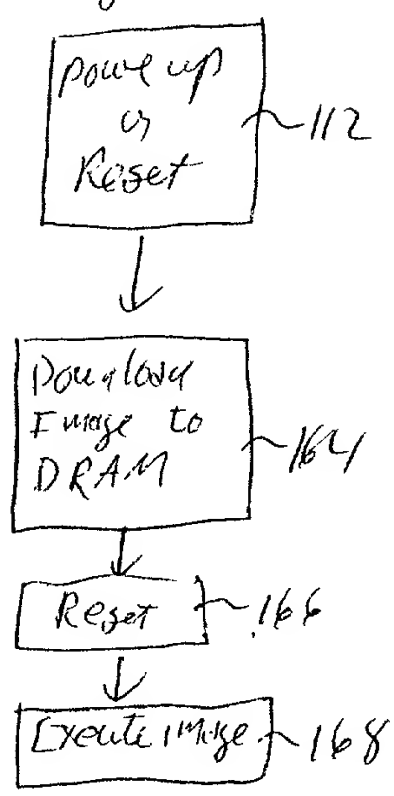


Fig. 1D
Prior Art

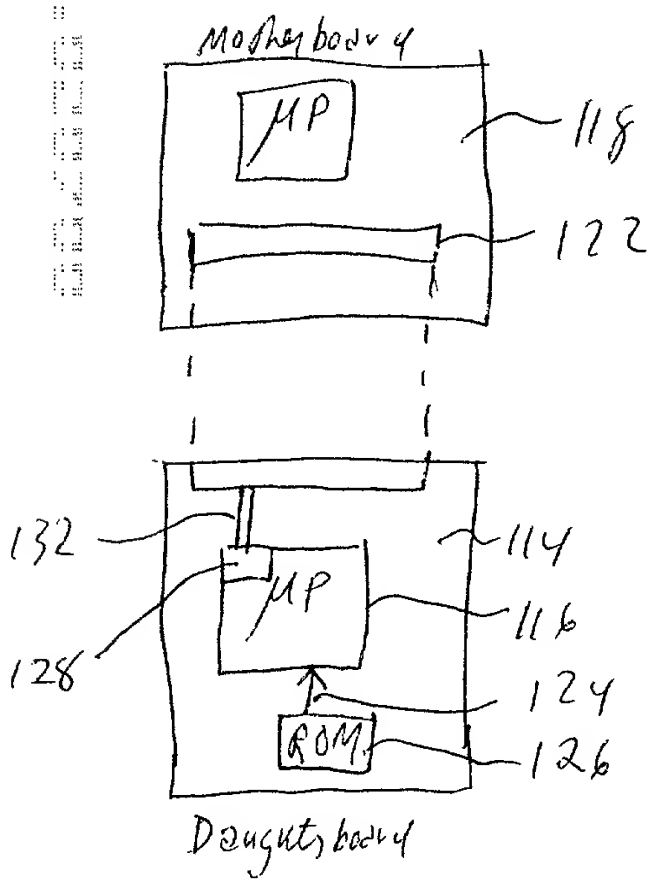


Fig 1E
Prior Art

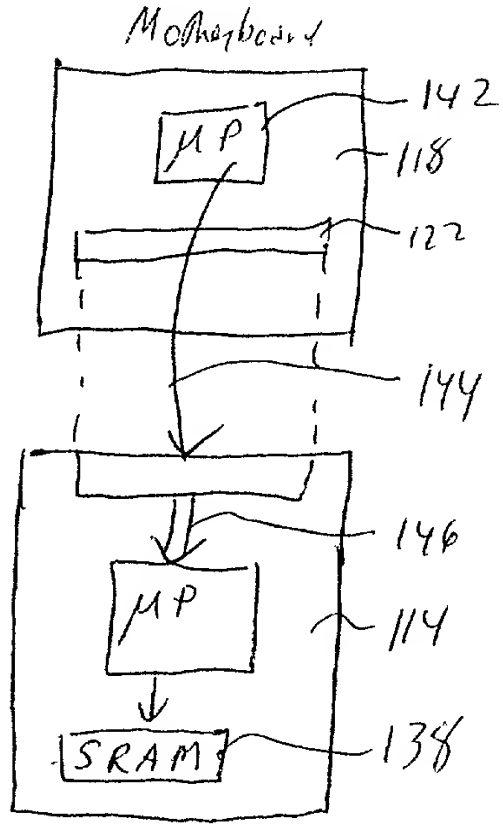
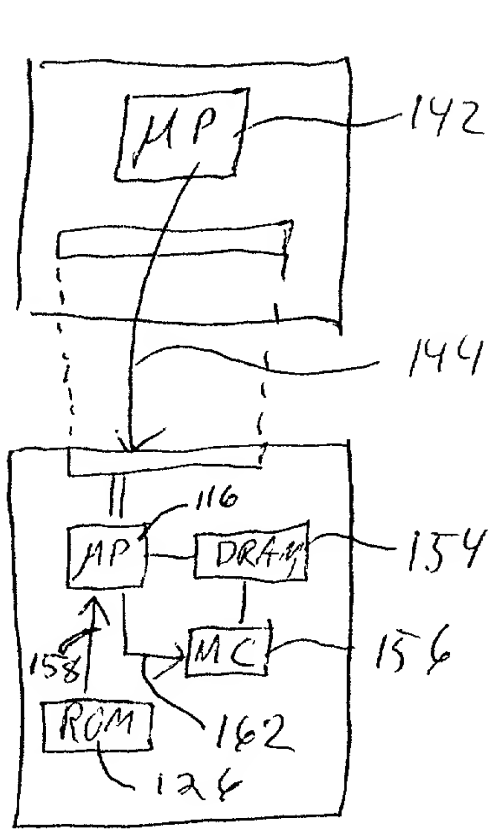
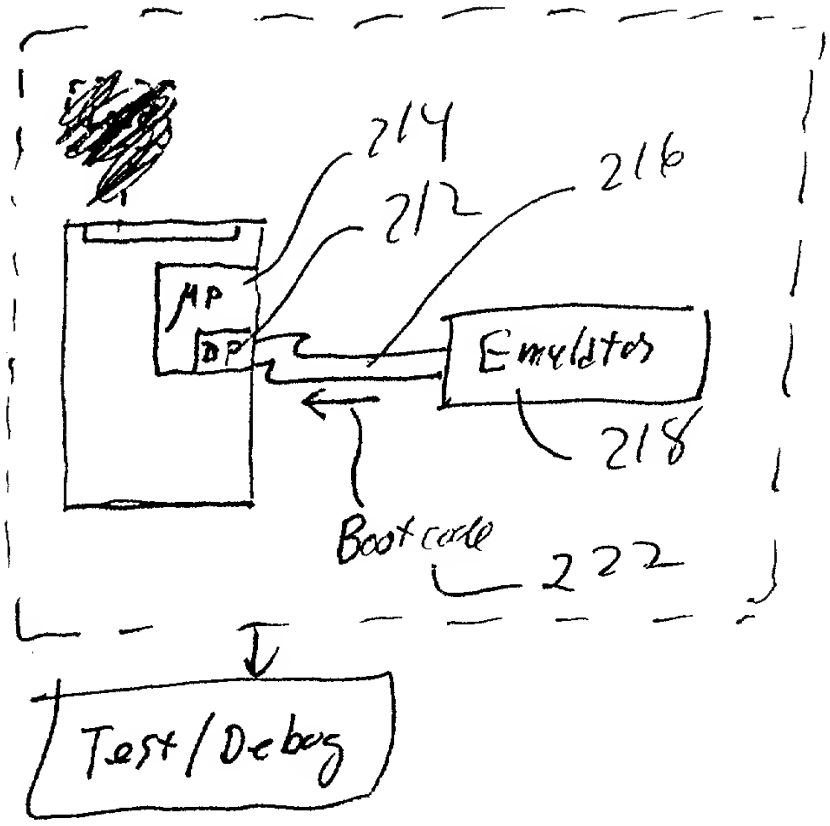


Fig 1F
Prior Art





Prior Art

Fig 2

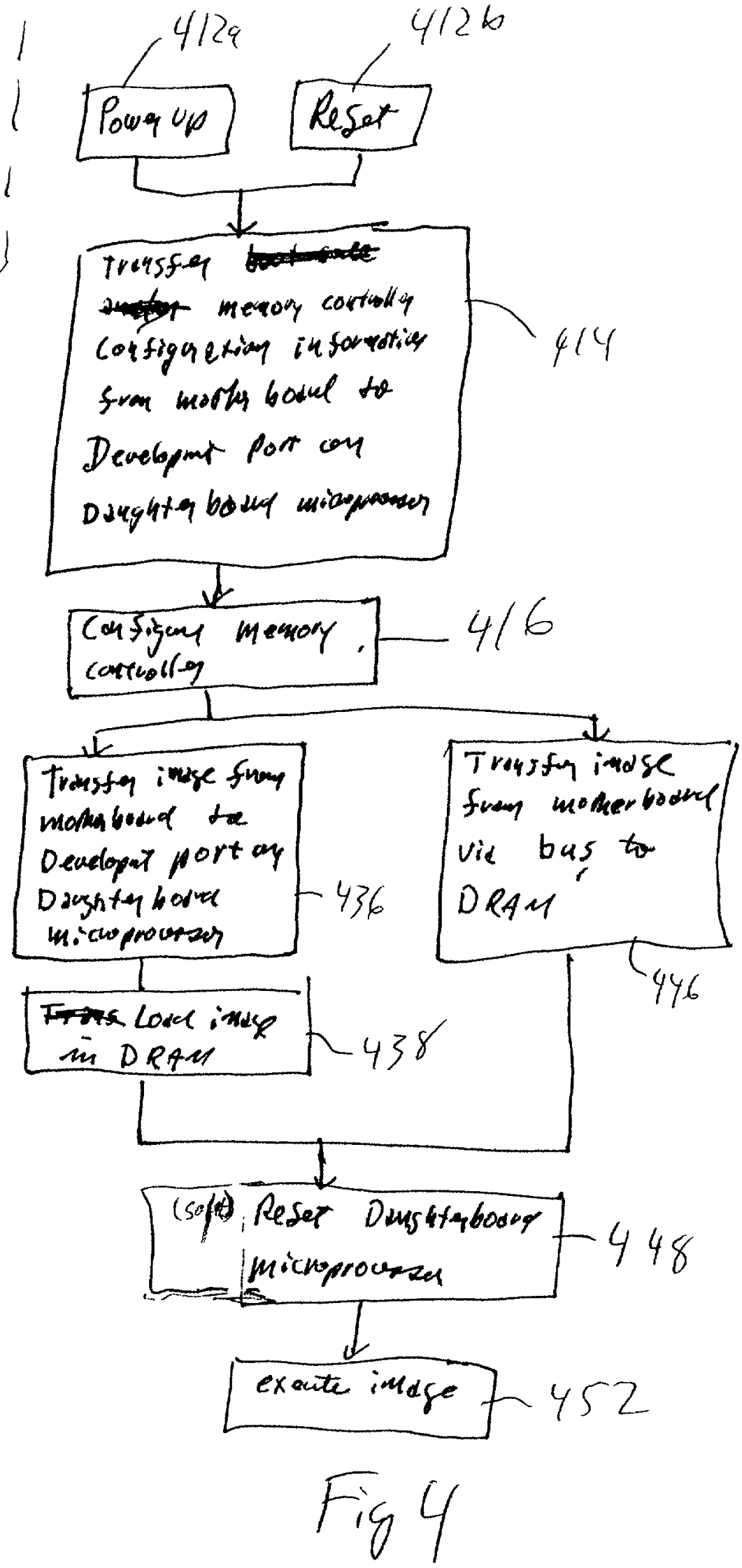


Fig 4

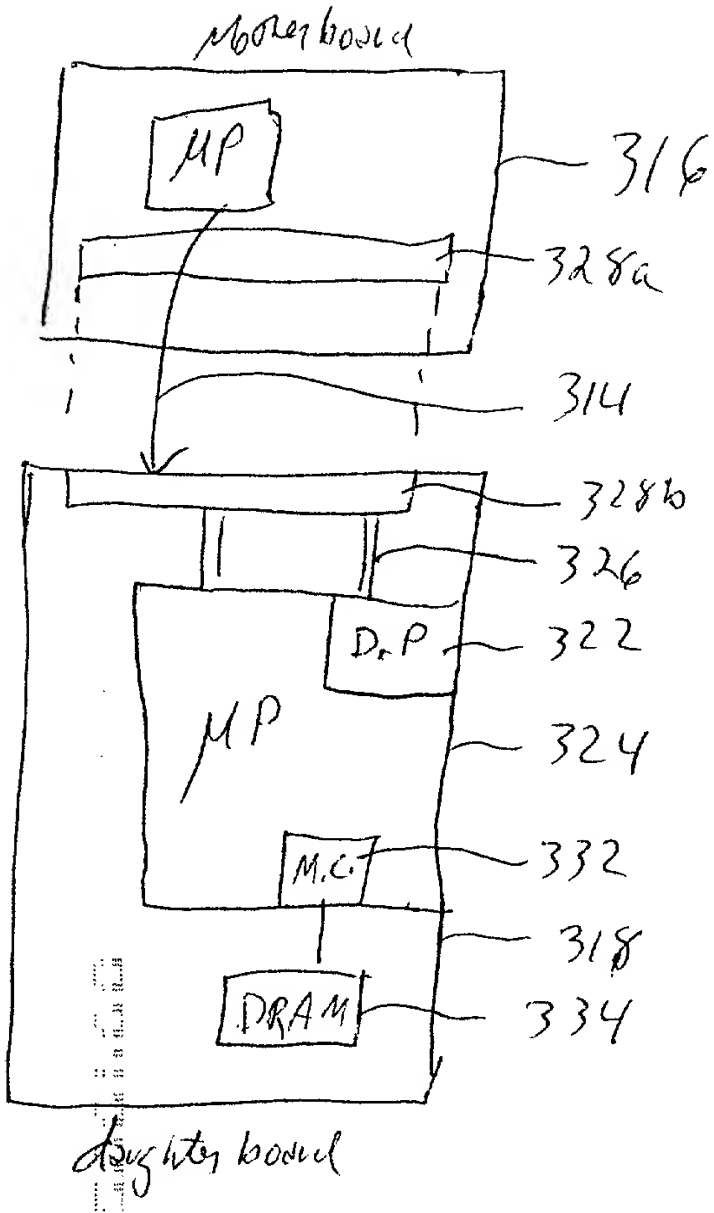


Fig 3A

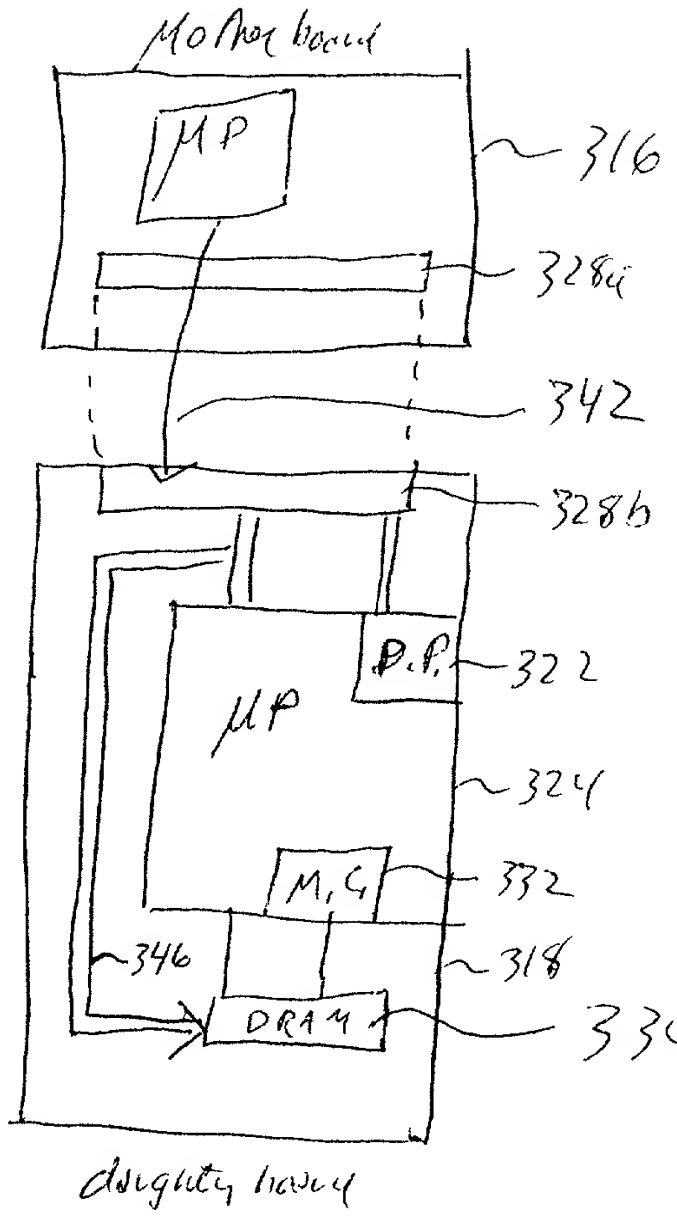


Fig 3B

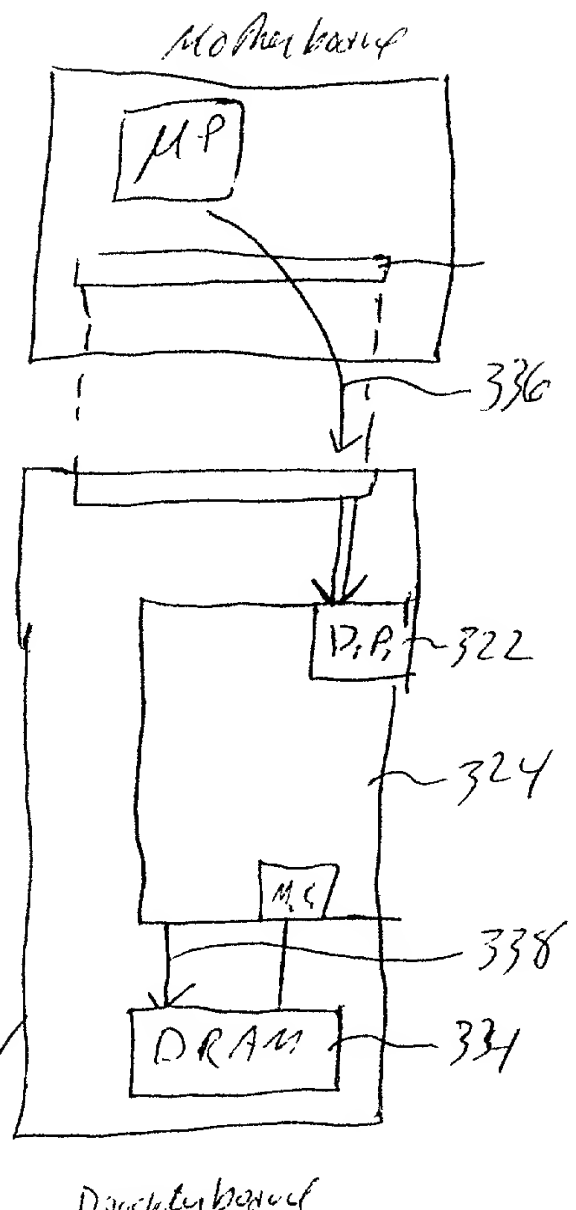


Fig 3C

RULE 63 (37 CFR § 1.63)
DECLARATION
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND APPARATUS FOR USING A DEVELOPMENT PORT FOR BOOT UP, the specification of which is identified as Attorney File No. 4103-40821 and attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability in accordance with 37 CFR 1.56(a) and (b) as set forth on the attached sheet indicated Page 3 hereof and which I have read.

I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No

I hereby claim the benefit under 35 U.S.C. 120/365 of all United States and PCT international applications listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information material to patentability in accordance with 37 CFR 1.56(a) and (b) which occurred between the filing date(s) of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: patented, pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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37 CFR §1.56(a) and (b)
DUTY TO DISCLOSE INFORMATION MATERIAL
TO PATENTABILITY

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of a patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.*

*Note, 37 CFR §1.97(h) states: "The filing of an information disclosure statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56(b)."